RELEASED

RFLM-011014QC-290

Wei Bo Associates HK Limited

Quasi Active High Power L-Band PIN Diode Limiter Module - SMT

Features:

- Frequency Range: 1.0 to 2.0 GHz
- High Peak Power Handling: +56 dBm
- High Average Power Handling: +56 dBm
- Low Insertion Loss (1.2 - 1.4 GHz): <0.15 dB
- Return Loss (1.2 - 1.4 GHz): >24 dB
- Low Flat Leakage Power : <17 dBm
- Low Spike Energy Leakage: <0.5 ergs
- SMT Package: 8mm x 5mm x 2.5mm
- DC Coupling Capacitors
- No external control lines or power supply required
- RoHS Compliant

Description:

The RFLM-011014QC-290 SMT Silicon PIN Diode Limiter Module offers both High Power CW and Peak protection in the L-Band region. It is based on a proven hybrid assembly technique utilized extensively in high reliability, mission critical applications. The RFLM-011014QC-290 offers excellent thermal characteristics in a compact, low profile 8mm x 5mm x 2.5mm package. The RFLM-011014QC-290 is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the L-Band frequency range.

The limiter RF circuit characteristics provide outstanding passive receiver protection (always on) which protects against High Average Power up to +56 dBm, High Peak Power up to +56 dBm pulsed, maintains low flat leakage to less than 17 dBm, and reduces Spike Leakage to less than 0.5 ergs.

ESD and Moisture Sensitivity Rating

The RFLM011014QC-290 Limiter Module carries a Class 1A ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

The RFLM-011014QC-290 based substrate has been designed to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat Au embrittlement concerns. Also, a proprietary design methodology has minimized the thermal resistance from the PIN Diode junction to base plate. The two stage limiter design employs a second stage Schottky and quarter wavelength spacer detector circuit which permits ultra-fast turn on of the High Power PIN Diodes. This circuit topology coupled with the thermal

characteristic of the substrate design enables reliably handling High Input RF Power up to 53dBm CW and RF Peak Power levels up to 55 dBm (3 ms pulse width @ 10% duty cycle with base plate temperature at 85°C).

Absolute Maximum Ratings

@ Zo=50Ω, T_A= +25°C as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	T_{CASE}=+55°C, source and load VSWR < 1.2, RF Pulse width = 100 us, duty cycle = 10%, derated linearly to 0 W at T_{CASE}=150°C (See note 1)	56 dBm
RF CW Incident Power		56 dBm
RF Input & Output DC Block Capacitor Voltage Breakdown		100 V DC

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

RFLM011014QC-290 Electrical Specifications

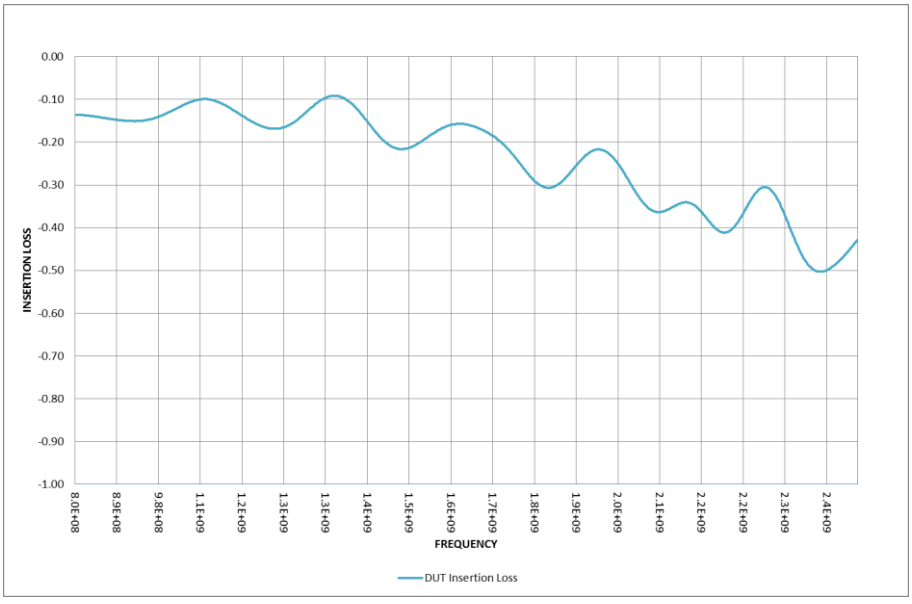
@ Zo=50Ω, TA= +25°C as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	1 GHz ≤ F ≤ 2 GHz	1		2	GHz
Insertion Loss	IL	P_{in}= -20 dBm, F = 1.0 - 2.0 GHz		0.15	0.3	dB
Insertion Loss Rate of Change vs Operating Temperature	ΔIL	1 GHz ≤ F ≤ 2 GHz, Pin ≤ -10 dBm		0.005		dB/°C
Return Loss	RL	Pin= -20 dBm, F = 1.0 -2.0 GHz	17	24		dB
Input 1 dB Compression Point	IP_{1dB}	1 GHz ≤ F ≤ 2 GHz		10		dBm
2nd Harmonic	$2F_o$	P_{in}= 0 dBm, F_o= 2.0 GHz		-50	-45	dBc
Peak Incident Power	$P_{inc\ (PK)}$	RF Pulse = 100 usec, duty cycle = 10%, t_{rise} ≤ 2us, t_{fall} ≤ 2 usec			56	dBm
CW Incident Power	$P_{inc(CW)}$	1 GHz ≤ F ≤ 2 GHz			56	dBm
Flat Leakage	FL	P_{in} = 56 dBm, RF Pulse width = 100 us, duty cycle = 10%, t_{rise}≤ 2 us, t_{fall}≤ 2 us		17	19	dBm
Spike Leakage Power	SLP	Pin = 56 dBm, RF Pulse width = 100 us, duty cycle = 10%		20		dBm
Spike Leakage Energy	SLE	Pin = 56 dBm, RF Pulse width = 100 us, duty cycle = 10%		0.5	0.6	erg
Recovery Time	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = 56 dBm peak, RF PW = 100 us, duty cycle = 10%, trise ≤ 2us, t_{fall} ≤ 1 usec		1.5		usec

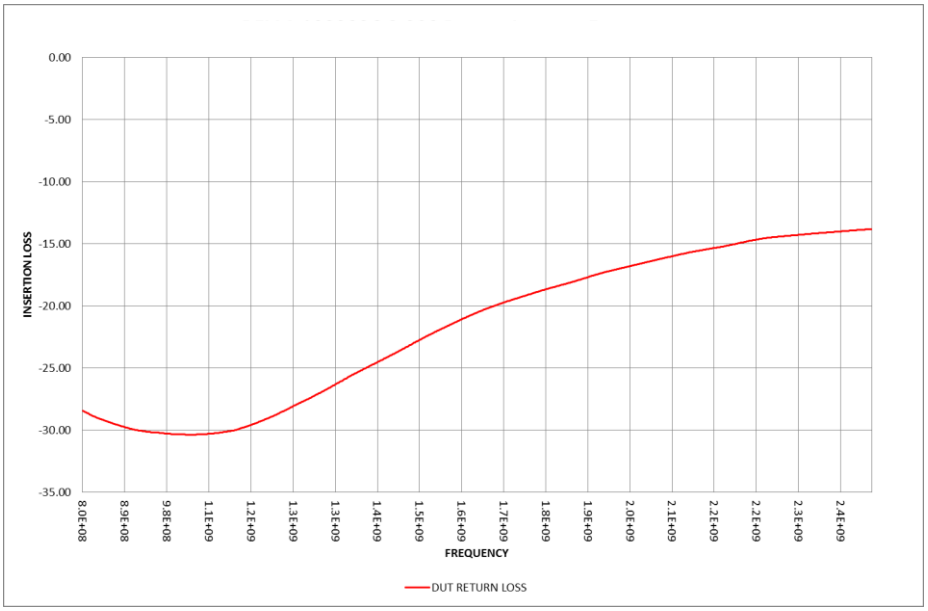
RFLM-011014QC-290 Typical Performance

Z_o = 50Ω, T_{CASE} = +25°C, PIN = -20 dBm as measured on the Ground Plane of the device.

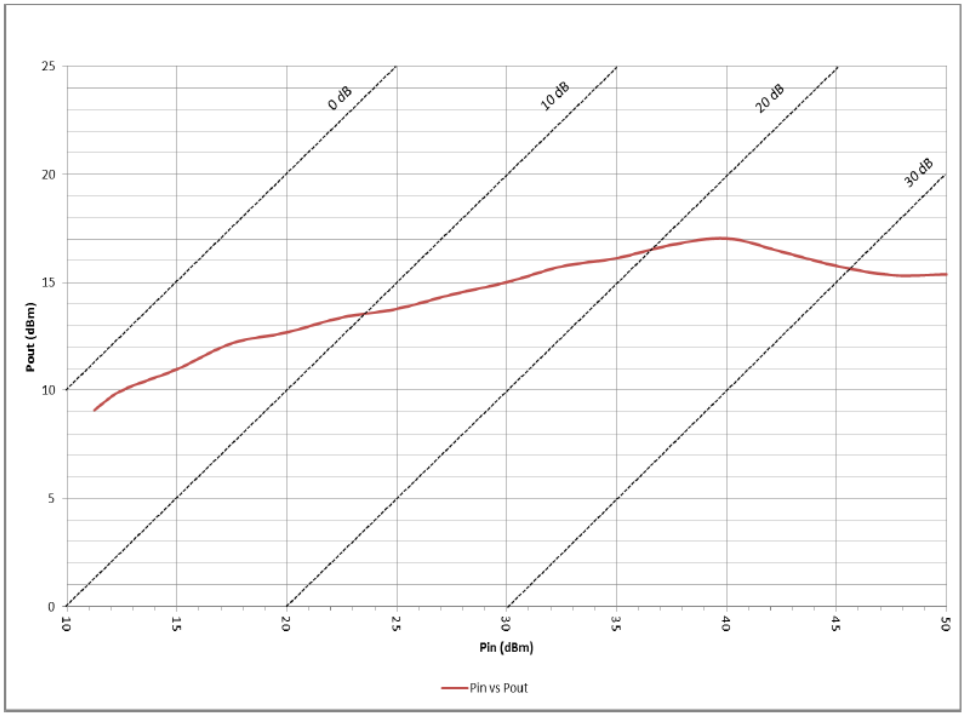
RFLM-011014QC-290 Insertion Loss vs Frequency



RFLM-011014QC-290 Return Loss vs Frequency

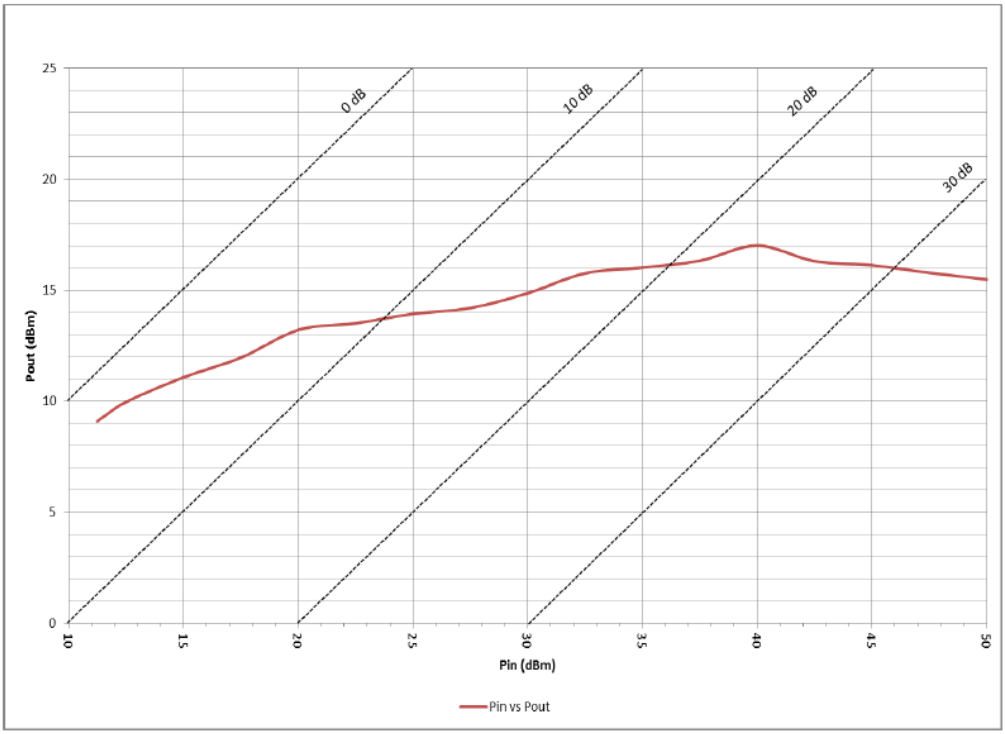


RFLM-011014QC-290 Flat Leakage: Input Power vs Output Power, CW, 2GHz



RFLM-011014QC-290 Flat Leakage Output Power vs Input Power

Pulse Width = 10 usec; Duty Cycle = 1%; F = 2 GHz

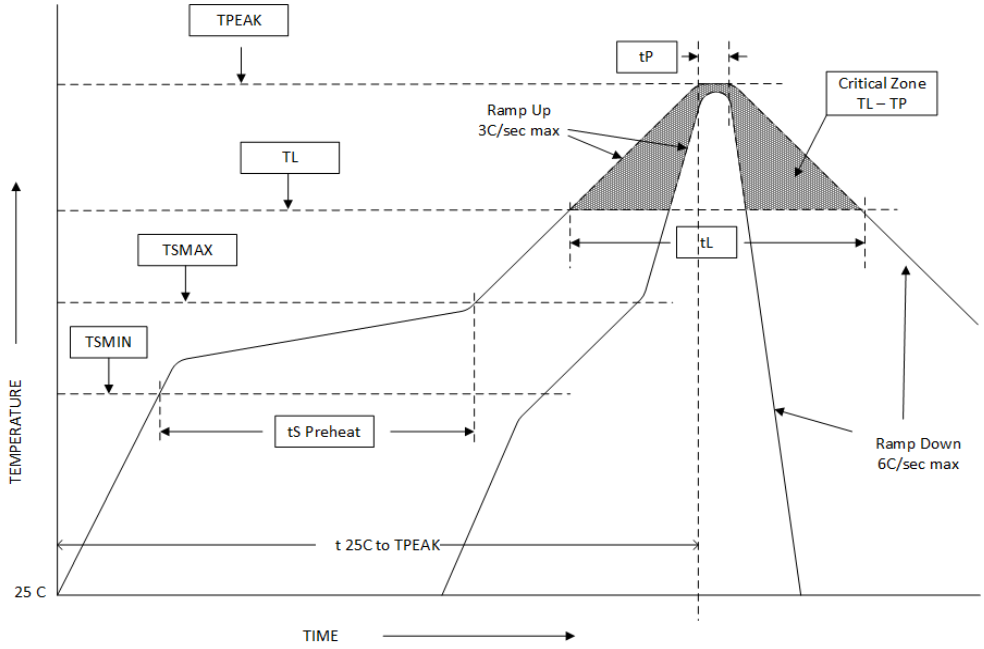


Assembly Instructions

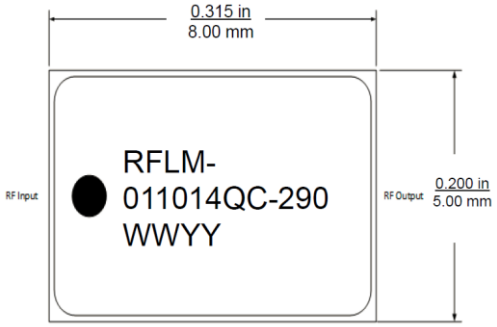
The RFLM-011014QC-290 may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

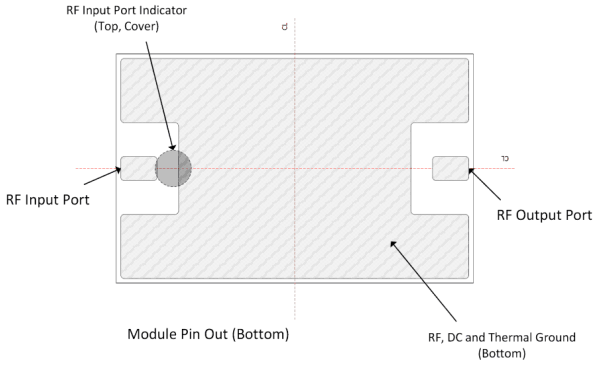
Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60 – 120 sec	 100°C 150°C 60 – 120 sec
T_{smax} to T_L Ramp up Rate		3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



RFLM-011014QC-290 Limiter Module Package Outline Drawing





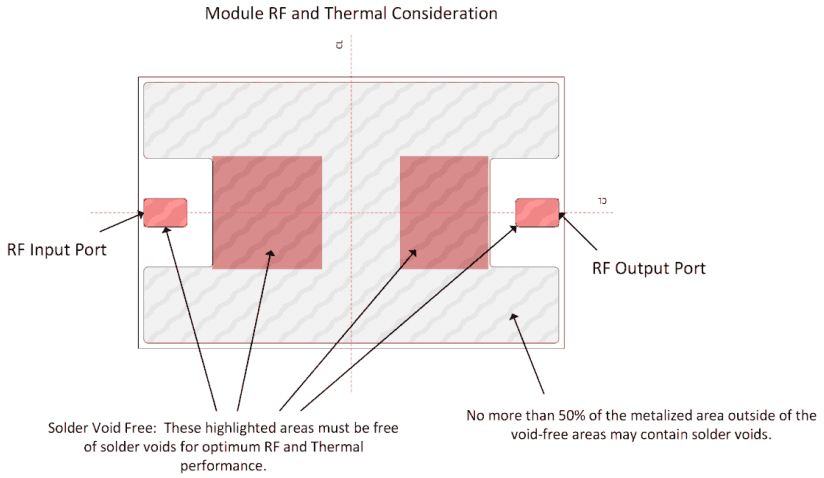
Notes:

1) Metalized area on backside is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (Au plated over Cu).

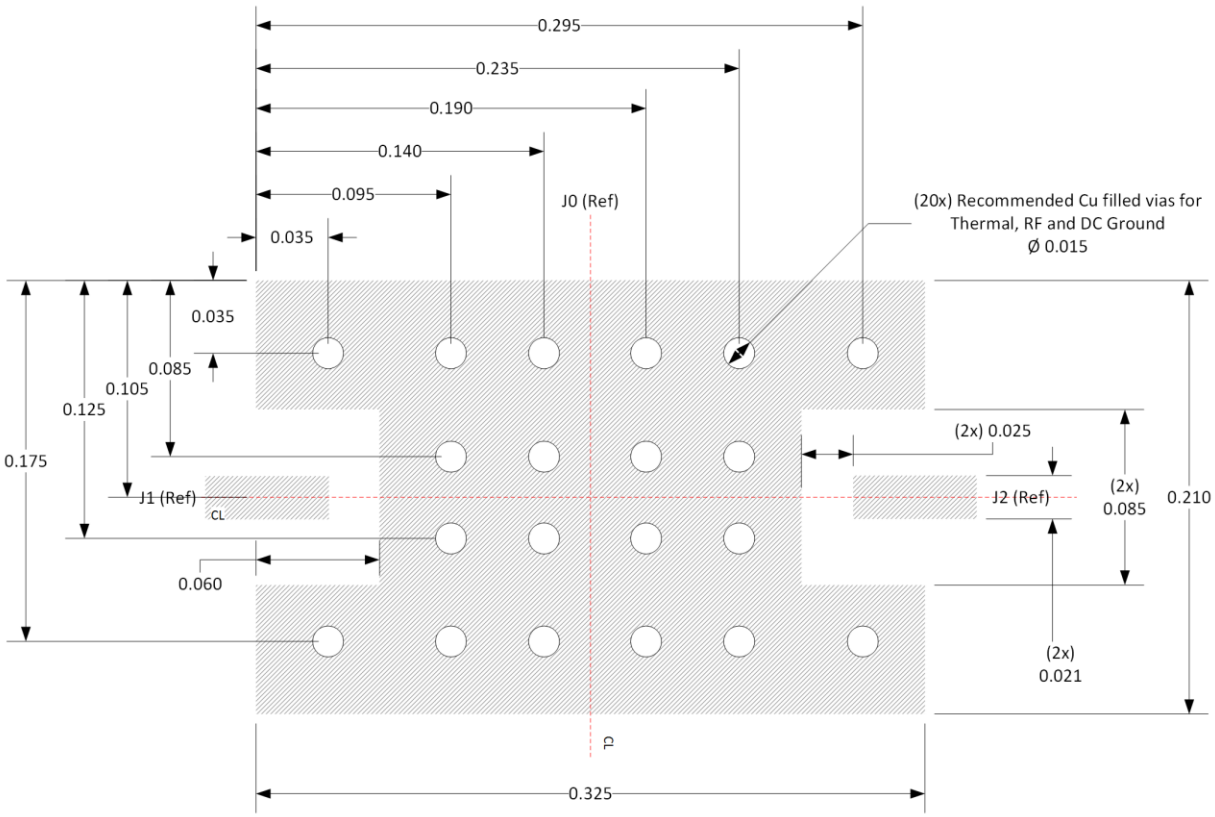
Thermal Design Considerations:

The design of the RFLM-011014QC-290 family of Limiter Modules permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than 55ºC.

There must be a minimal thermal and electrical resistance between the limiter bottom surface and ground. Adequate thermal management is required to maintain a T_{JC} at less than +175ºC and thereby avoid adversely affecting the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the area shaded in red in the figure shown below:



Recommended RF Circuit Solder Footprint for the RFLM011014QC-290



Notes:

1) Recommended PCB material is Rogers 4350B, 10 mils thick (RF Input and Output trace width needs to be adjusted from the recommended footprint.)
2) Hatched area is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.

Part Number Ordering Detail:

The RFLM-011014QC-290 Limiter Module is available in the following format:

Part Number	Description	Packaging
RFLM-011014QC-290	L-Band Limiter, Input & Output DC Blocking Caps	Gel-Pack
RFLM-011014QC-290 SS EVB	RFLM-011014QC-290 Small Signal Evaluation Board	Box
RFLM-011014QC-290 HP EVB	RFLM-011014QC-290 High Power Evaluation Board	Box
RFLM-011014QC-290C	RFLM-011014QC-290 SMA Connectorized	Box